RELIASIC (2014-2018)
Reliable ASIC
« Energy and resource efficiency in ICT »

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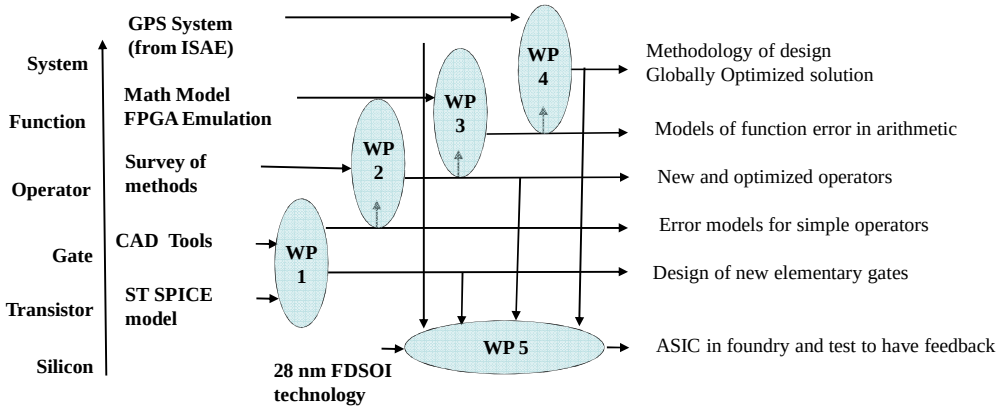
Context

- **Nanoscale systems are becoming more and more sensitive to process, voltage and temperature (PVT) variations:** Process variations are attributed to the imperfections in the manufacturing process.
- PVT variations can significantly affect the performance and behavior of circuits. Therefore it is increasingly important to deal with different effects of these variations.
- **Fault tolerant computing** : The art and the science of building computing systems that continue to work properly in the presence of faults due to PVT variations.

Objectives

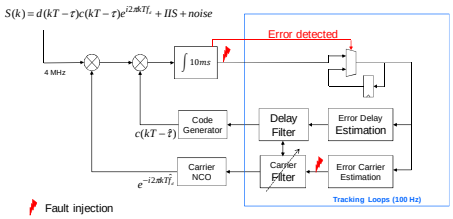
- Reduce the power consumption of embedded systems
- Address the problem of fault tolerant computation by studying the case of an existing application (a GPS receiver).
- Produce two versions of the application on an ASIC (using a 28 nm CMOS technology) : a standard GPS receiver and a hardened GPS receiver tolerant to faults due to low voltage supply.

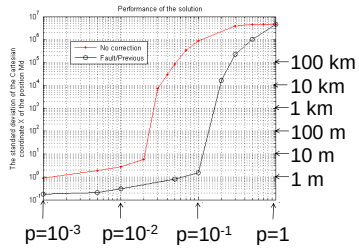
Structure of RELIASIC



First results

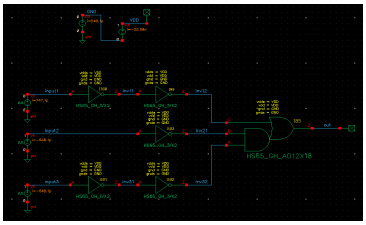
- Adding some mechanisms to allow the tracking module of the GPS receiver to be more tolerant to faults in the integrator and the carrier discriminator.

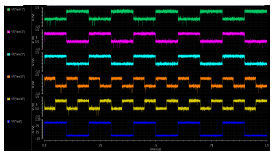


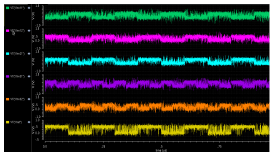


- 10^{-1} Error probability
  - direct implementation
    => error of 1000 km
  - smart implementation
    => error of 1 m

- Modelling of Random Telegraph Noise inside a circuit.







Simulation Conditions:
- Temperature = 27°C
- Input Clock Frequency = 5MHz and 10MHz
- Process: 65nm, Nominal

Vin = VSUPPLY = 1 Volt

Vin = VSUPPLY = 0.5 Volt

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